REMARKS

This amendment is submitted in response to the Examiner's Action dated May 8, 2003. Applicants have amended the claims herein to more clearly and completely recite features of the invention, which are described in the specification. No new matter has been added, and the amendments place the claims in condition for allowance. Applicants respectfully request entry of the amendments to the claims. Where arguments are provided below to rebut claim rejections, those arguments are in reference to the claims in their amended form.

CLAIMS REJECTIONS UNDER 35 U.S.C. § 102

At paragraph 4 of the Office Action, Claims 1-2, 5-6 and 9 are rejected under 35 U.S.C. § 102(e) as being taught by Morris, et al. (U.S. Patent No. 6,079,012). Morris does not anticipate Applicants' invention because Morris does not teach each element recited within Applicants' amended claims.

Applicants' claimed invention now recites: "an **in-order** processor that issues **all** memory access requests in program order, wherein said processor ...accepts data retrieved by a first and a second memory access request into its execution units only in said program order" and a controller ... which **automatically** places a barrier operation ... following each issuance of a memory access request to said memory system, wherein said barrier operation indicates a need to complete the data operations associated with the memory access requests in program order from the perspective of the processor." All memory access requests as recited by Applicants includes all read requests and write requests.

Morris, in contrast with Applicant's claimed invention does not issue ALL memory access requests in program order or automatically place a barrier operation following issuance of EACH memory access request. Examiner cites to specific sections of Morris, which provide a processor that (1) sometimes operates in-order for some instructions and (2) which only orders similar memory access operations with each other (i.e., reads with reads and writes with writes). With respect to the first limitation, Morris at col. 3, line 65 – col. 4, line 2 specifically states the computer executes programs "in an ordered way **when required**." Thus, as further chown with respect to the second limitation, Morris places the control after a read or write operation in

specific situations, and NOT after every/each memory access request. Col. 7, lines 33-67 supports only this very specific load-with-load, write-with-write limitation of Morris. That section describes not allowing a load instruction to complete before prior load instructions complete and then not allowing a write instruction to complete before prior write instructions complete.

This distinction is extremely important as Applicants' invention ensures correct dependencies between writes and reads of the same memory location, which Morris appears to not be concerned about.

The standard for a § 102 rejection requires that the references teach each element recited in the claims set forth within the invention. As clearly outlined above, the references each fail to meet this standard and therefore do not anticipate Applicants' invention.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103(a)

At paragraph 11 of the Office Action, Claims 3-4, 7-8 and 10-11 are rejected under 35 U.S.C. § 103(a), as being unpatentable over Morris, et al. (U.S. Patent No. 6,079,012) as applied to Claims 1, 5 and 9 above, in view of Karp, et al. (U.S. Patent No. 6,321,328). The arguments proffered above, which clearly show that the independent claims are allowable over Morris also overcome the present rejection of their dependent claims.

Nevertheless, Applicant would further show that the combination of Karp with Morris does not render the above claims unpatentable since Karp (and thus the combination) does not suggest the specific features that are provided by these claims. Examiner appears to rely on Karp's reference to the term "speculative" in concluding that Karp provides the "speculative issuing of load instructions" as that phrase is recited within Applicants' specification and claims.

As utilized and/or defined by Applicants, speculative issuing of load requests refer to the fact that the load request may actually return data that may be changed or invalidated by a previously issued memory access request. This scenario occurs when the subsequently issued load request completes (i.e., returns data from memory) before a previously issued write request

completes in the memory, potentially affecting the very line of data that was thus "speculatively" loaded.

In contrast to Applicants use of the term, Karp specifically indicates that the term "speculative" refers only to the fact that the load request may not actually be required to be completed because of a branch instruction preceding it in the instruction sequence, which may take a different path from which the load is in (see col.1, lines 41-60). Karp's utilization of the term speculative is therefore not synonymous with Applicants' use of the term, and Applicants specific use of the term is functionally distinct and would not be obvious in light of Karp.

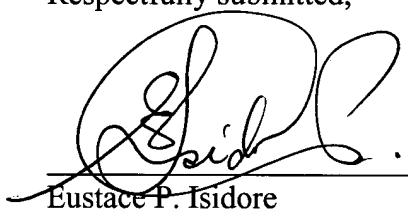
For these reasons, one skilled in the art would not find Applicants invention obvious in light of the combinations. The above claims are therefore allowable.

CONCLUSION

Applicants have diligently responded to the Office Action by amending the claims to more clearly recite the features unique to Applicants' invention. Applicants have further shown why the claims are not taught by nor unpatentable over the cited references. The amendments and arguments overcome the §102 and §103 rejections, and Applicants, therefore, respectfully request reconsideration of the rejections and issuance of a Notice of Allowance for all claims now pending.

Applicants request the Examiner contact the undersigned attorney of record at (512) 542-2100 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,



Eustace P. Isidore
Registered with Limited Recognition (see attached)
BRACEWELL & PATTERSON, L.L.P.
P.O. Box 969
Austin, Texas 78767-0969
(512) 542-2100
ATTORNEY FOR APPLICANT(S)